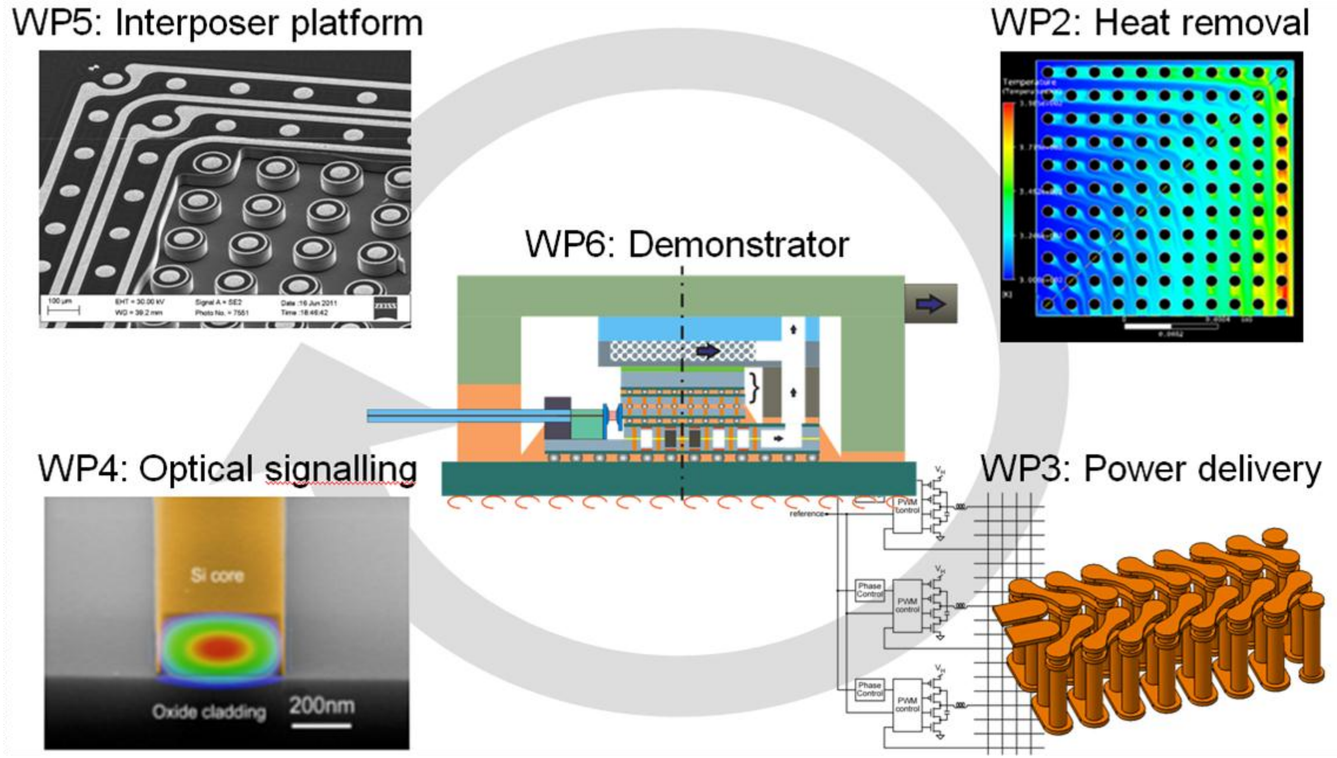
CarrICool: Interposer supporting optical signaling, liquid cooling, and power conversion for 3D chip stacks

Project info

- EU FP7 project
  - Project: 619488
- Begin: Jan. 2014
- End: Dec. 2016



Project partners

IBM

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Tyndall National Institute

ipdia The 3D Silicon Leader

optocap

Fraunhofer

TECHNISCHE UNIVERSITÄT CHEMNITZ

AMIC

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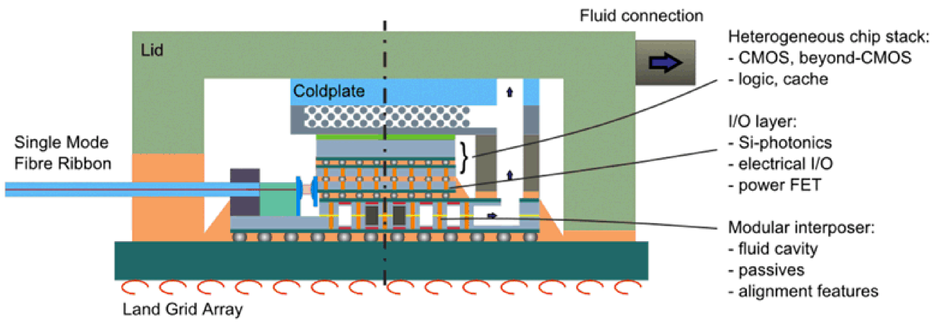
CarrICool project objectives

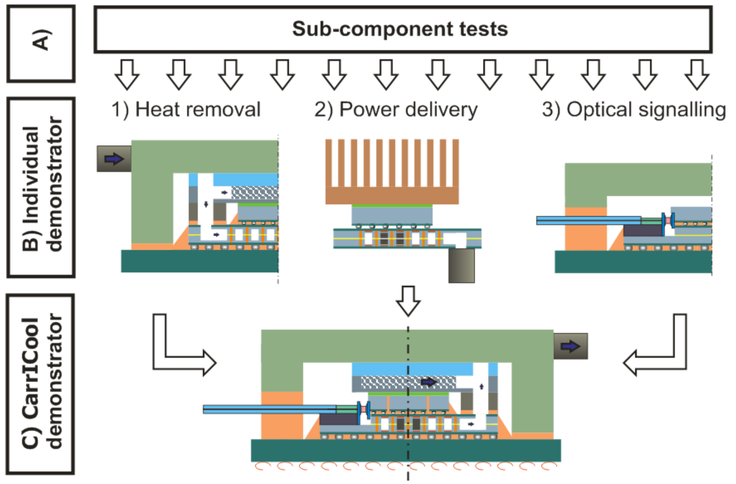
Functional interposer

- Power conversion
- Optical signaling
- Liquid cooling

CarrICool target demonstrator



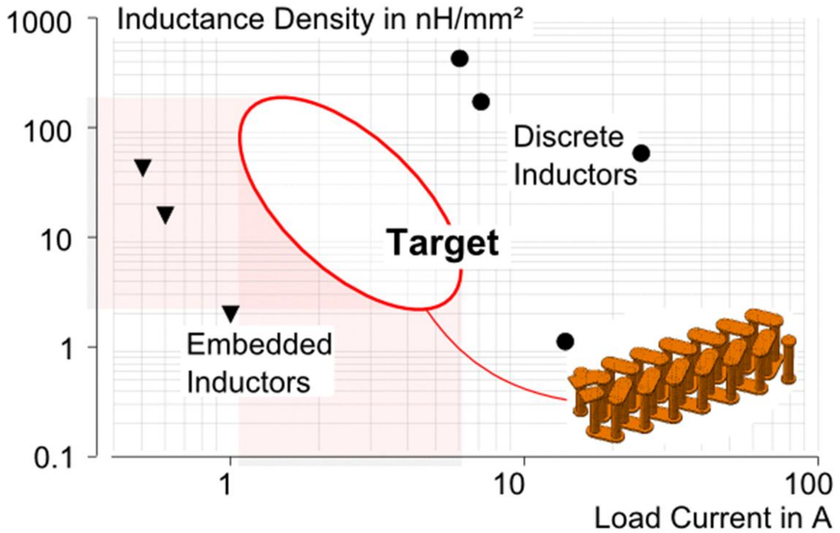
Development phases



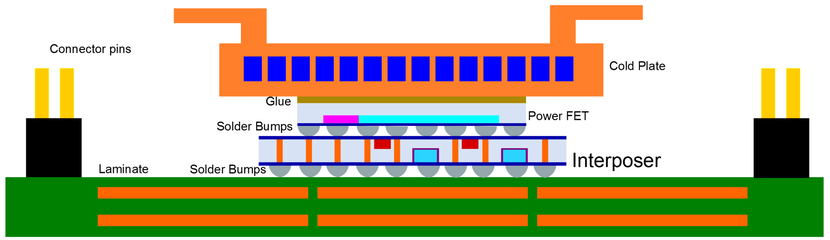
Power converter (iVRM)

- Deep submicron technology
- L and C on interposer
- Switches and control on CPU

TSV inductors



iVRM demonstrator



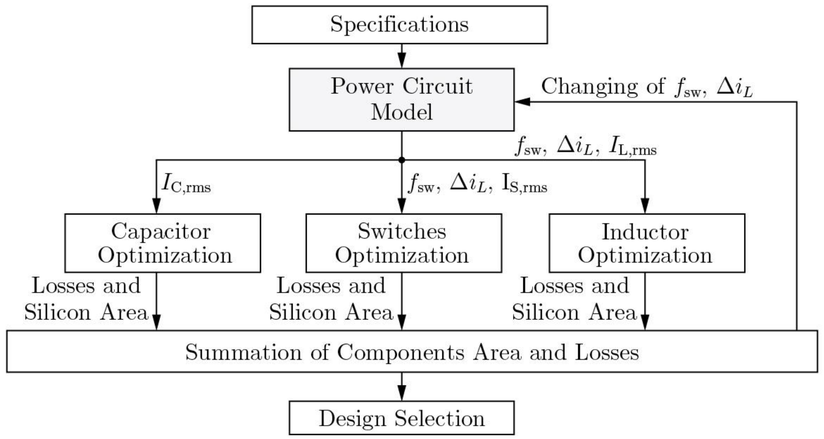
Power management IC – 32nm vs 14nm SOI CMOS

Converter specifications

Parameter	Specifications for 14nm implementation
V_{in} [a]	1.7V
V_{out} [b]	0.6V to 1.1V
Efficiency [c]	90%
PMIC power density [d]	30W/mm^2
Interposer power density [e]	4W/mm^2
$V_{out,ripple}$ (steady state)	10mV
$V_{out,droop}$ (transient) [f]	10mV

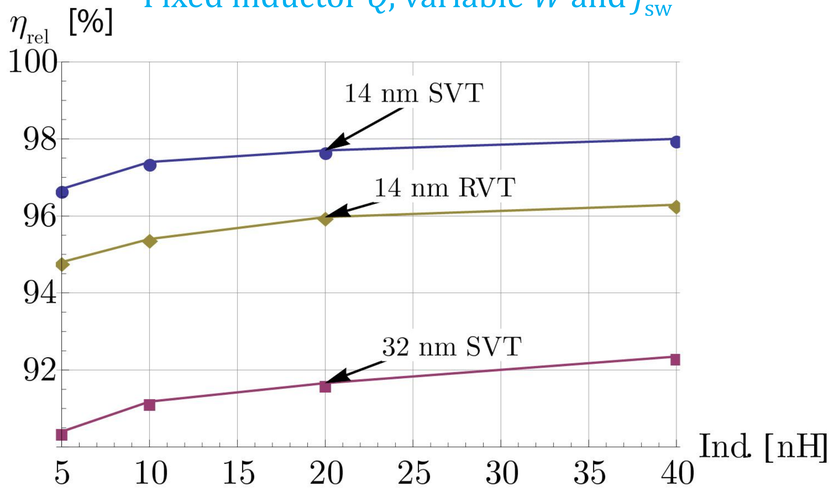
- [a] Nominal output voltage is $V_{out,nom}$=850mV. Nominal V_{in} is twice $V_{out,nom}$.
- [b] Variable output voltage to support DVFS
- [c] Maximum efficiency to be optimized for full load assuming high CPU utilization application
- [d] Corresponding to <1% CPU area
- [e] CPU power density is assumed to be 2W/mm^2. Allowing 50% interposer area to passives gives 4W/mm^2 interposer power density.
- [f] Transient load conditions are 50% -> 100% $I_{out,max}$ load step in 5ns

Optimization procedure

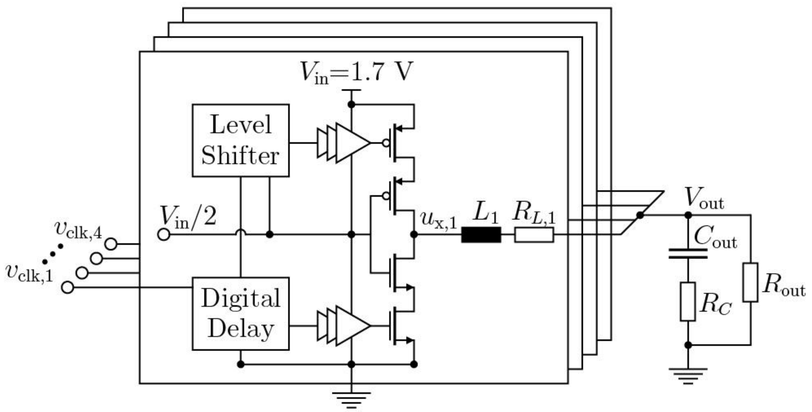


Without inductor losses

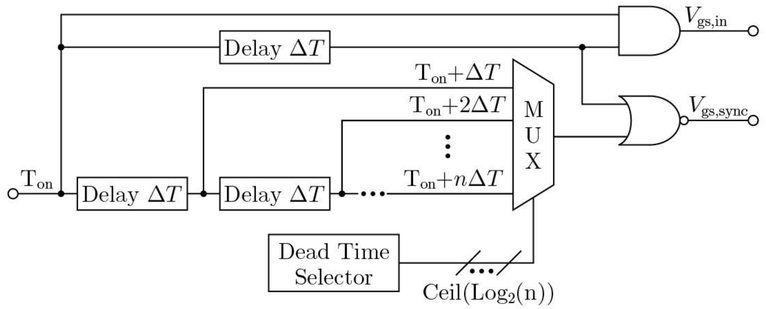
Fixed inductor Q, variable W and f_{sw}



Buck converter

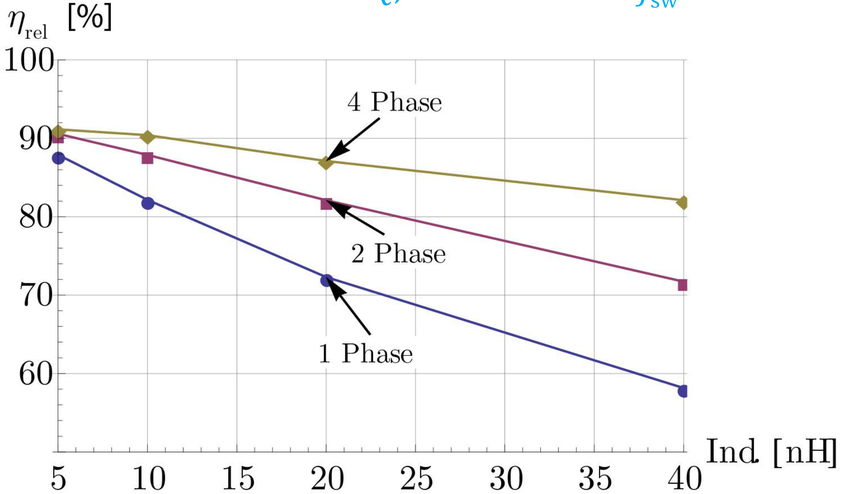


Adaptive deadtime



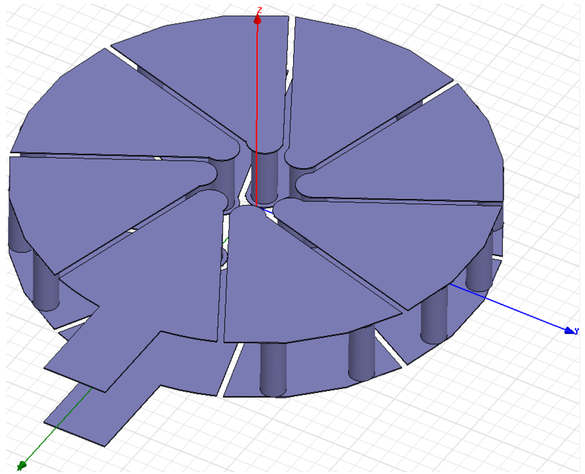
With inductor losses

Fixed inductor Q, variable W and f_{sw}

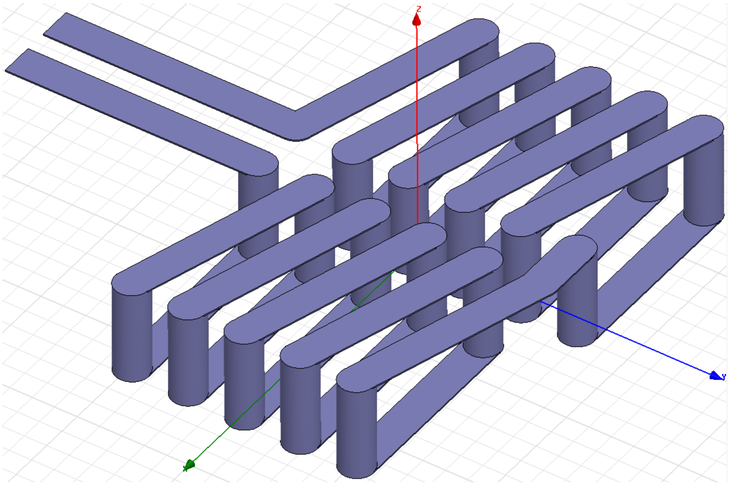


TSV inductor structures and modeling

Toriodal inductor structure



Helical inductor structure



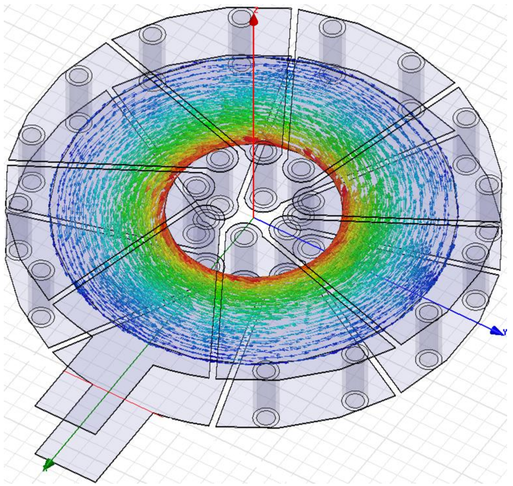
Modeling results - inductance

Comparison of analytical model and FEA simulation at 50 MHz
(2 µm thick flat core)

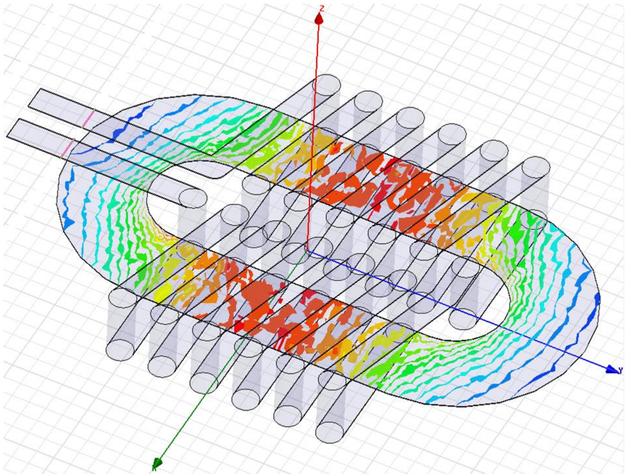
TOROIDAL INDUCTOR				
	Air core		Magnetic flat core	
Turn number	Calculation (nH)	Maxwell (nH)	Calculation (nH)	Maxwell (nH)
12	6.571	6.607	26.249	26.095
8	3.707	3.787	14.289	14.27

HELICAL INDUCTOR				
	Air core		Magnetic flat core	
Turn number	Calculation (nH)	Maxwell (nH)	Calculation (nH)	Maxwell (nH)
12	9.167	9.078	25.674	26.58
10	7.508	7.509	20.175	20.831
8	5.886	5.901	14.943	15.318
6	4.294	4.324	10.067	10.255

Toriodal with core material



Helical with core material



Modeling results – resistance

Comparison of analytical model and FEA simulation
TSV diameter: 75 µm (half filled vias)
TSV spacing: 50 µm
TSV depth: 200 µm
Cu thickness: 3 µm

TOROIDAL INDUCTOR		
	R_{dc}	
Turn number	Calculation (mΩ)	Maxwell (mΩ)
12	381	385
12 (10um Cu)	133	138
8	226	218
8 (10um Cu)	80	84

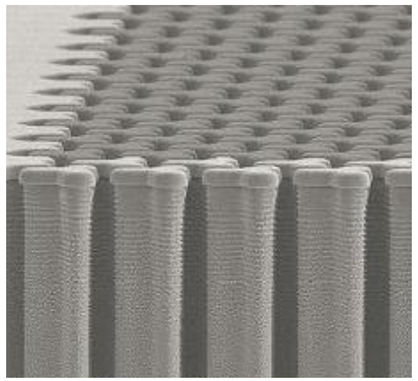
HELICAL INDUCTOR		
	R_{dc}	
Turn number	Calculation (mΩ)	Maxwell (mΩ)
12	817	805
10	695	693
8	573	572
6	451	452

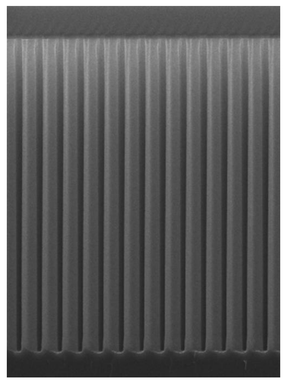
Optimized inductance density for 1 mm^2 > 30 nH/mm^2
L/DCR > 0.8 nH/mΩ

Deep trench capacitors

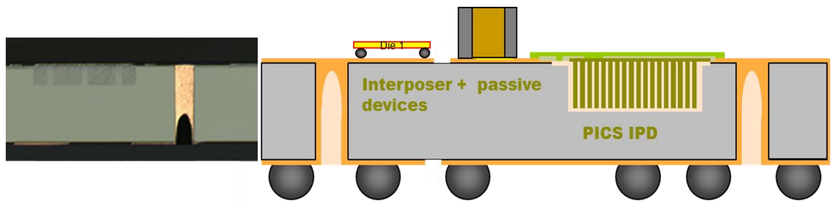
Deep trench capacitors

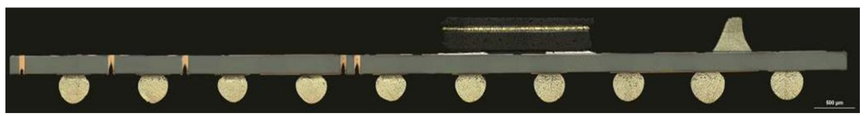
- Capacitor density up to 500nF/mm^2
- Low leakage current < 1nA/µF, FIT << 1
- Excellent temperature and voltage linearity
- Low ESR & low ESL



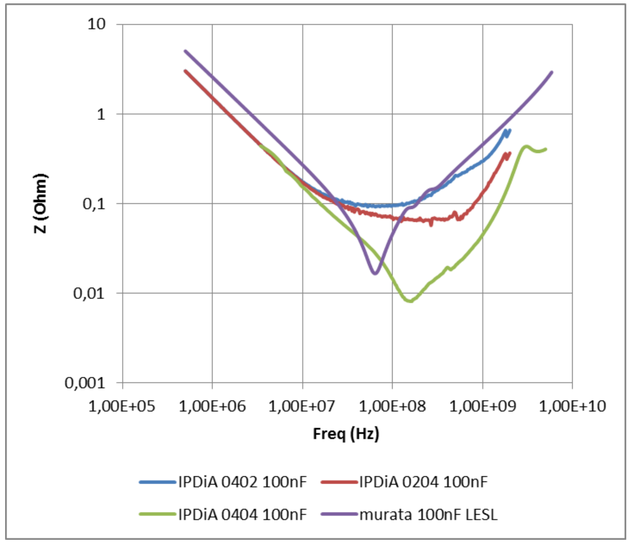


3D Capacitors + TSV

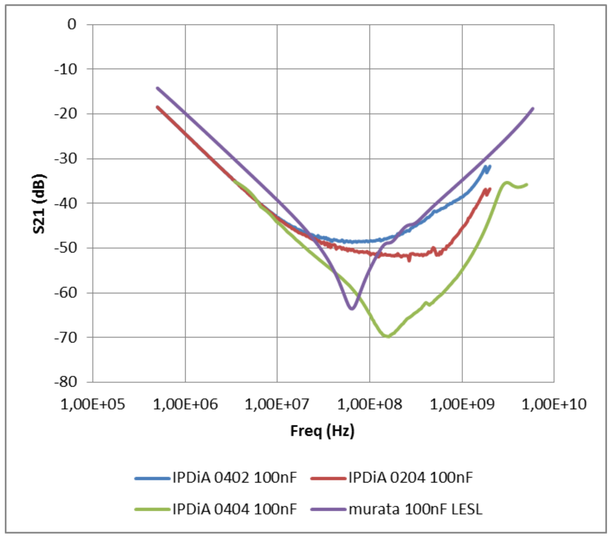




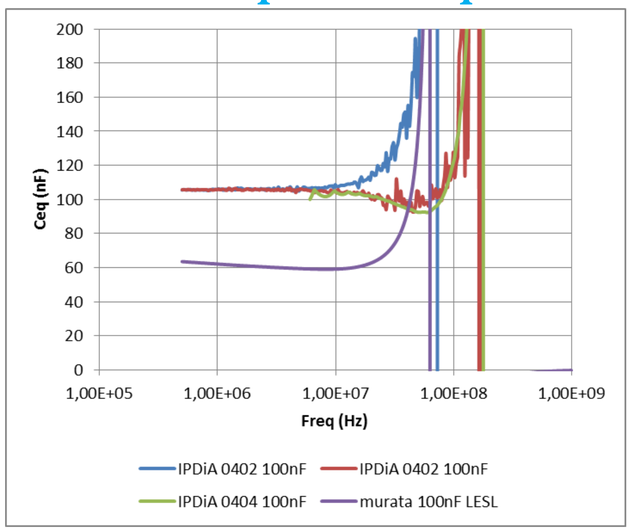
Z vs Freq



S21 vs Freq



Ceq vs Freq



Leq vs Freq